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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/603,749	SCHRADER ET AL.	
	Examiner	Art Unit	
	IAN N. MOORE	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 February 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *2/1/08* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 6-12 are objected to because of the following informalities:

Claim 6 recites "**a plurality of subcomponents**" in line 2-3. For consistency and clarification with "**multiple subcomponents**" recited in claim 1, line 5, it is suggested to change "**a plurality of subcomponents**" in line 2-3, to "the **plurality of subcomponents**" or "**the multiple subcomponents"**.

Claim 8 recites "**a plurality of subcomponents**" in line 2-3. For consistency and clarification with "**multiple subcomponents**" recited in claim 1, line 9, it is suggested to change "**a plurality of subcomponents**" in line 2-3, to "the **plurality of subcomponents**" or "**the multiple subcomponents"**.

Claim 10 recites "according to **one** claim 8" in line 1. For clarification, it is suggested to remove "one".

Claims 7, 13-15, 9, and 12 are also objected since they are depended upon objected claims 6 and 8 as set forth above.

Appropriate correction is required.

Specification

2. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required:

Claim 1 recites, "subcomponent being designed to process the time-synchronous data in **a specific and different way**" in line 6-7 and "subcomponent being designed to process the time-synchronous data in **a specific and different way**" in lines 10-11. The specification fails to provide proper antecedent basis for subcomponents (i.e. CODEC 6a, FILTER 6b and PACKTIZER 6c) of first processing unit 3 and subcomponents (i.e. CODEC 6a', FILTER 6b' and PACKTIZER 6c') of second processing unit 4 are designed to process "specifically" and "differently".

Claim Rejections - 35 USC § 112 – First Paragraph

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 13 and 14 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. (*NOTE- these issues have been raised in previous office action*).

Claim 13 recites, "after switching by the switch, the subcomponents of the first processing unit are **de-attached from each other**" in line 1-2.

The specification fails to disclose how subcomponents (see FIG. 3, 6a', 6b', 6c') of processing unit 3 are de-attached after switching to processing unit 4. In other word, CODEC 6a', FILTER 6b' and PACKTIZER 6c' in the processing unit 3 are disconnected to each other

after switching. The specification page 6-7 repeatedly discusses processing unit 3 and unit 4 are performing parallel by togging the switch between processing units in order to adapt to the changed data rate network characteristic. It is unclear how CODEC 6a', FILTER 6b' and PACKTIZER 6c' disconnected from each other after switching. Are they are actually removed? How does the disconnection occur between CODEC, FILTER and PACKTIZER? How does the processing unit 3 operate after essential components such as CODEC, FILTER and PACKTIZER are de-attached (e.g. processing time sensitive data packet without CODEC, FILTER, or PACKTIZER)? How disconnected CODEC, FILTER and PACKETIZER can perform parallel processing, if they are disconnected? What is the relationship between the resources and subcomponents? How do the subcomponents de-attached after switching with regards to resources?

Applicant responded to this issue by referring to the specification recites on page 7, lines 27-28 that "***The switch can hereby be realized as hardware or software***", and arguing that "as would be clearly understood by those of ordinary skill in the art, disconnection (and re-connection) of the codec, filter and packetizer could also be realized with either hardware or software switches".

Examiner respectively disagrees with the applicant argument. One skilled in the ordinary art would see that by disclosing the switch is "hardware" or "software" in the specification clearly is not enabling disclosure for the claimed invention "**after switching by the switch, the subcomponents of the first processing unit** (i.e. CODEC, FILTER and PACKETIZER) **are de-attached from each other**"

1) since "the switch" and "CODEC, FILTER and PACKETIZER" separated components, and thus having a hardware or software "switch" has nothing to do with "CODEC 6a, FILTER 6b and PACKETIZER 6c" are de-attached/disconnect from each other. Clearly, one skilled in the ordinary would not know how to de-attached/disconnect CODEC 6a, FILTER 6b and PACKETIZER 6c from each other after the switch without enabling disclosure;

2) As shown in applicant specification FIG. 3, after switching by switch 5 from the first processing unit 3 to the second processing unit 4, the switch is now connecting with the second processing unit 4. Thus, it is also clear that having a hardware or software "switch" has nothing to do with "CODEC 6a, FILTER 6b and PACKETIZER 6c" in the first processing unit 3 since the switch is not even connected to "CODEC 6a, FILTER 6band PACKETIZER 6c" after switching to second processing unit 4. Clearly, one skilled in the ordinary would not know how to de-attached/disconnect CODEC 6a, FILTER 6b and PACKETIZER 6c of first processing unit 3 from each other when the switch is not even connected to them without enabling disclosure.

Since the applicant argued that "as would be clearly understood by those skilled in the art", it clear that applicant is admitting the specification fails to support enabling disclosure for the claimed invention. Examiner agrees with the applicant admission since applicant referred page and lines or any other pages fail provide enabling support for the claimed invention.

As set forth above, the claimed invention would not be clearly understood by those skilled in the art. The arguments of counsel cannot take the place of evidence in the record (see MPEP 716.01(c) II).

Since applicant fails to clearly point out the enabling reference in the specification where the claimed invention is supported, and the claimed invention would not be clearly understood

by those skilled in the art, examiner sustains the assumption, for the purpose of the examination, "in light of the applicant disclosure" *that after switching, the first processing subcomponents (6a', 6b',..) are de-attached/separated from the second processing subcomponents (7a', 7b',...).*

Claim 14 recites, "**the** subcomponents of the first processing unit **are included in one of the second processing units**" in line 2-4.

The specification fails to disclose how subcomponents (see FIG. 3, 6a', 6b', 6c') of processing unit 3 are included in the processing unit 4 after switching by the switch. Per FIG. 3, the processing unit 4 already has subcomponent CODEC 7a, FILTER 7b and PACKETIZER 7c, and then one of CODEC 6a, FILTER 6b and PACKETIZER 6c is included in the second processing unit. It is unclear how the second processing unit uses two CODECs, two FILTERs, or two PACKTIIZER. How does one process using one of CODEC 6a, FILTER 6b and PACKETIZER 6c, with existing CODEC 7a, FILTER 7b and PACKETIZER 7c? How do they integrate? The specification page 6-7 repeatedly discusses processing unit 3 and unit 4 are performing parallel by togging the switch between processing units in order to adapt to the changed data rate network characteristic. It is unclear what kind of parallel processing can possible done when CODEC 6a, FILTER 6b and PACKETIZER 6c in the processing unit 3 is included in the processing unit 4. What is the relationship between the resources and subcomponents? What resources which are not currently being used returned to the system for re-use? What is the system- processing unit 1 or 2? How does resource reuse by the system?

Applicant argues that "claim recites is "a plurality of the second processing units" and that "the subcomponents of the first processing unit are included in one of the second processing units…claim quite clearly contemplates a plurality of second processing unit and when the

subcomponents of the first processing unit are incorporated into one of the second processing units, one of ordinary skill in the art would understand that parallel processing is performed by at least two of the plurality of second processing units".

First, applicant misunderstood the rejection since the issue is, as precisely stated, "**the** subcomponents of the first processing unit (i.e. CODEC 6a, FILTER 6b and PACKETIZER 6c) **are included in one of the second processing units (i.e. second processing unit 4)** while at least one of the second processing units 4 already has it own subcomponents (i.e. CODEC 6a, FILTER 6b and PACKETIZER 6c). Clearly, one skilled in the ordinary would not know how to incorporate CODEC 6a, FILTER 6b and PACKETIZER 6c from first processing unit 3 to at least one of the second processing units 4 without enabling disclosure.

Since the applicant argued that "as would be clearly understood by those skilled in the art", it clear that applicant is admitting the specification fails to support enabling disclosure for the claimed invention. Examiner agrees with the applicant admission since applicant referred page and lines or any other pages fail provide enabling support for the claimed invention.

As set forth above, the claimed invention would not be clearly understood by those skilled in the art. The arguments of counsel cannot take the place of evidence in the record (see MPEP 716.01(c) II).

In view of the above, it is clear that applicant fails to clearly point out the enabling reference in the specification where the claimed invention is supported, and the claimed invention is not clearly understood by those skilled in the art.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 1-4 and 6-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zahn (WO 00/62254) in view of Sastry (US006694373B1).

Regarding Claim 1, Zahn discloses an apparatus (see FIG. 1,2; apparatus 1) for the transmission of time-synchronous data (see FIG. 3, video signal 50; see page 4, paragraph 3-8; see page 9, last paragraph; real time/synchronous video signal utilizing MPEG or HDTV) from a sender to a receiver using a network (see page 4-6; a video signal must transmit from a transmitter to a receiver/customer over a network), wherein the time-synchronous data is processed and transmitted at the sender as well as the receiver (see FIG. 1, 2,4,5, the video data is processed at transmitter or receiver/customer; see page 9, last paragraph), the mechanism comprising:

a first processing unit (see FIG. 1, 2,4,5, a combined system of Processor CPU 5 and memory 6; see page 9, last paragraph) composed of multiple subcomponents (see FIG. 1,2,4,5, CPU 5 and memory 6), each subcomponent being designed to process the time-synchronous data in a specific and different way (see FIG. 1,2,4,5, CPU 5 process the video signal in specific/particular and different/dissimilar way/method (e.g. processing of video data signal) from memory 6, and memory 6 process the video signal in specific/particular and

different/dissimilar way/method (e.g. storing the video data signal) from CPU 5; see page 9, last paragraph);

a second processing unit parallel to the first processing unit (see FIG. 1,2, 4,5, a combined system of Processor CPU 5' and memory 6', where a combined system of CPU 5 and memory 6 is parallel to a combined system of CPU 5' and memory 6'; see page 9, last paragraph; see page 11, paragraph 1-2; see page 12, paragraph 2 to page 13, paragraph 2), composed of multiple subcomponents (see FIG. 1,2,4,5, CPU 5' and memory 6'), each subcomponent being designed to process the time-synchronous data in a specific and different way (see FIG. 1,2,4,5, CPU 5' process the video signal in specific/particular and different/dissimilar way/method (e.g. processing of video data signal) from memory 6', and memory 6' process the video signal in specific/particular and different/dissimilar way/method (e.g. storing the video data signal) from CPU 5'; see page 9, last paragraph; see page 11, paragraph 1-2; see page 12, paragraph 2 to page 13, paragraph 2);

wherein the subcomponents of second processing unit are setup and adapted based on changed sender data rate or network characteristics (see page 4, paragraph 3-4, page 8, paragraph 3-7; page 11, paragraph 1 to page 12, paragraph 3; see page 13, paragraph 5-6, last paragraph; CPU 5' and memory 6' are setup and fit/adapted for parallel storage and processing according to sender/transmitter/source increasing/changing real time data rate (i.e. data rate 4 or 8 times/factor of 25/30 frames/second that carriers high resolution format), or real time data load or bandwidth/delay (i.e. network characteristic)) by configuring attribute parameters of the subcomponents (see page 4, paragraph 3-4, page 8, paragraph 3-7; page 11, paragraph 1 to page

12, paragraph 3; see page 13, paragraph 5-6, last paragraph; by setting/configuring resolution format and latency/congestion of CPU 5' and storage/capacity/load of memory 6'),

wherein data processing and transmission of the time-synchronous data is continued within the first processing unit during the setup and adaptation of the second processing unit (see page 11, paragraph 1-3; processing and transmission of real time data packet (e.g. packet 101) is continued/parallel-processed in the CPU 5 while CPU 5' is setup and fit/adapted for parallel processing); and

selecting/switching between the first and second processing units (see FIG. 1, line 2, switching/changing/selecting between CPU 5 and CPU 5'; see page 9, last paragraph; see page 11, paragraph 1-2; see page 12, paragraph 2; see page 13, paragraph 4-5), the processing and transmission of the time-synchronous data initially being performed by the first processing unit (see FIG. 2, processing and transmission of real time data packet primarily/initially performed by the CPU 5; see page 9, last paragraph; see page 11, paragraph 1-2; see page 12, paragraph 2 to page 13, paragraph 2) and after switching (see FIG. 1-3, after switching/changing/selecting), the processing and transmission of the time-synchronous data is performed using the second processing unit (see FIG. 1-3, processing and transmission of real time data packet (e.g. continue data packet 102) is processed by CPU 5'; see page 4, paragraph 3-4, 8 page 8, paragraph 3-7; page 11, paragraph 1 to page 12, paragraph 3; see page 13, paragraph 5-6, last paragraph) such that the processing and transmission of the time-synchronous data is performed within the second processing unit (see FIG. 1-3, the pr processing and transmission of real time data packet (e.g. continue data packet 102) is processed by CPU 5'' see page 4, paragraph 3-4, 8 page 8,

paragraph 3-7; page 11, paragraph 1 to page 12, paragraph 3; see page 13, paragraph 5-6, last paragraph).

Although Zahn discloses changing/selecting/switching between the first processing unit and the second processing units, Zahn does not explicitly disclose "a switch".

However, it is well known in the art the selecting/changing/switching is performed by a switch/selector/changer. In particular, Sastry discloses an apparatus (see FIG. 2, server 220/230/260; see FIG. 3, server 310; see FIG. 4,6; server 405/605) for the transmission of time-synchronous data (see FIG. 2, real time data; see col. 3, line 29-31, 48-51, 62-67) from a sender (see FIG. 2, sending/transmitting client 241-244/251-254) to a receiver (see FIG. 2, receiving client 251-254/241-244) using a network (see FIG. 2, using network 210), wherein the data is processed and transmitted at the sender as well as the receiver (see FIG. 2,3,4,6, server 310 process and transmitted to sending client 241-244 as well as the receiving client 251-254; see col. 3, line 32 to col. 4, line 10) the mechanism comprising:

a first processing unit (see FIG. 4, DSP-S 431, see FIG. 6, DSP-S631, or see FIG. 8, DSP 801/802), and a second processing unit parallel to the first processing unit (see FIG. 4,6,8. DSP-D 439/639/803 parallel to DSP-S 431/631/801), wherein data processing and transmission of the time-synchronous data is continued within the first processing unit during the setup and adaptation of the second processing unit (see col. 4, line 32-60; see col. 5, line 12-20; processing and transmission of real time data is continued/process-parallel in the DSP-S 431/631/801 while setting-up/construction and adapting/configuring DSP-D 439/639/803 for parallel processing) and

a switch selecting between the first and second processing units (see FIG. 4,6, switch 420/620), the processing and transmission of the time-synchronous data initially being performed by the first processing unit (see FIG. 4,6, 8, processing and transmission of real time data primarily/initially performed by the DSP-S) and after switching by the switch (see FIG. 4, 6, 8, after switching by a switch 420/620; see col. 4, line 39-62; see col. 5, line 10-26, 36-56; see col. 6, line 12-20l; see col. 6, line 55 to col. 7, line 11), the processing and transmission of the time-synchronous data is performed using the second processing unit such that the processing and transmission of the time-synchronous data is performed within the second processing unit (see FIG. 4,6,8, processing and transmission of real time data is performed using the DSP-D (or any another DSP besides DSP-S) such that processing and transmission of the real time data is performed within DSP-D (or another DSP); see col. 4, line 39-62; see col. 5, line 10-26, 36-56; see col. 6, line 12-20l; see col. 6, line 55 to col. 7, line 11).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide a switch, as taught by Sastry in the system of Zahn, so that it would increase the support for the number of simultaneous calls/real-time data transmission and efficient resource allocation; see Sastry col. 3, line 15-30; see col. 7, line 5-12.

Regarding Claim 2, Zahn discloses wherein the setup and adaptation of the second processing is started using a trigger event (see FIG. 1, PULL request 1 is used to being processing video frames in CPU 5'; see page 11, paragraph 1-2; see page 12, paragraph 2; see page 13, paragraph 4).

Regarding Claim 3, Zahn discloses wherein the switching is performed after the completion of the setup and/or adaptation of the second processing unit (see FIG. 2,

switching/changing to CPU 5' after setup/configuration/setting CPU 5'; see page 9, last paragraph; see page 11, paragraph 1-2; see page 12, paragraph 2; see page 13, paragraph 4-5).

Regarding Claim 4, Zahn discloses wherein the switching is performed after reaching a certain switching condition (see FIG. 2, switching/changing to CPU 5' after frame 101 is processed by CPU 5; see page 9, last paragraph; see page 11, paragraph 1-2; see page 12, paragraph 2; see page 13, paragraph 4-5).

Regarding Claim 6, Zahn discloses wherein the time-synchronous data is processed in the first processing unit using a plurality of subcomponents (see FIG. 2, a first combined processing system comprising CPU 5 and memory 6; see page 12, paragraph 2).

Regarding Claim 7, Zahn discloses wherein the subcomponents includes at least one of a memory buffer (see FIG. 2, a first combined processing system comprising memory 6; see page 12, paragraph 2).

Regarding Claim 8, Zahn discloses wherein the time-synchronous data is processed in the second processing unit using a plurality of subcomponents (see FIG. 2, a second combined processing system comprising CPU 5' and memory 6'; see page 12, paragraph 2).

Regarding Claim 9, Zahn discloses wherein the subcomponents includes at least one of a memory buffer (see FIG. 2, a second combined processing system comprising memory 6'; see page 12, paragraph 2).

Regarding Claim 10, Zahn discloses wherein the subcomponents are connected during the setup (see FIG. 2, CPU 5' and memory 6' are connected during the configuration/setups; see page 9, last paragraph; see page 11, paragraph 1-2; see page 12, paragraph 2; see page 13, paragraph 4-5).

Regarding Claim 11, Zahn discloses wherein the first and second processing unit is initialized after the setup (see FIG. 2, a combined system of CPU 5/5' and memory 6/6' initialized/started/begin processing after the configuring/setting-up the each pipeline connections 1; see page 9, last paragraph; see page 11, paragraph 1-2; see page 12, paragraph 2; see page 13, paragraph 4-5).

Regarding Claim 12, Zahn discloses wherein each of the subcomponents of the second processing unit is adapted to the other subcomponents (see FIG. 2, CPU 5' and memory 6' of the combined system of CPU 5' and memory 6' is adapted/fit/adjust/corresponds to other CPU 5/5" and memory 6/6"; see page 12, paragraph 2), or the changed data rate, or changed network characteristics (see page 8, paragraph 3-7; page 11, paragraph 1 to page 12, paragraph 3; see page 13, paragraph 5-6; parallel processing accommodate/conform to the network dynamic/change nature of real time data rate or bandwidth/delay (i.e. network characteristics)).

Regarding Claim 13, Zahn discloses wherein after the switching process, the subcomponents of the first processing unit are de-attached from each other (see FIG. 2, after switching/changing to CPU 5', CPU 5 and memory 6 are separated/de-attached from CPU 5' and memory 6; see page 9, last paragraph; see page 11, paragraph 1-2; see page 12, paragraph 2; see page 13, paragraph 4-5).

Regarding Claim 14, Zahn discloses a plurality of the second processing units is setup and after switching by the switch (see FIG. 2, a second combined system of CPU 5' and memory 6' and a third combined system of CPU 5" and memory 6" are configured/setup, and after switching by the switch); and the subcomponents of the first processing unit (see FIG. 2, a first combined processing system comprising CPU 5 and memory 6; see page 12, paragraph 2). Sastry

discloses a plurality of the second processing units is setup (see FIG. 8, DSP 803,504,805,806 are setup/configured/constructed) and after switching by the switch after switching by the switch, the subcomponents of the first processing unit are included in one of the second processing units (see FIG. 8, after switching by a switch 420/620, subcomponent 2 ADPCM (Adaptive Pulse Code Modulation for voice compressing) from DSP 801 (i.e. first processing unit) are now included in the DSP 803; see col. 6, line 55 to col. 7, line 10).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to subcomponents of the first processing unit are included in one of the second processing units, as taught by Sastry in the system of Zahn, for the same motivation as set forth above in claim 1.

Regarding Claim 15, Zahn discloses wherein after switching by the switch, the subcomponents of the first processing unit remain connected (see FIG. 2, after switching/changing to CPU 5', CPU 5 and memory 6 are still connected; see page 9, last paragraph; see page 11, paragraph 1-2; see page 12, paragraph 2; see page 13, paragraph 4-5).

Regarding Claim 16, Zahn discloses wherein a plurality of second processing units (see FIG. 2, a combined system of 5" and memory 6", and more pipelines 1) are setup and adapted based on changed data load and network characteristics (see page 9, last paragraph; see page 11, paragraph 1-2; see page 12, paragraph 2; see page 13, paragraph 4-5; third combined system of 5" and memory 6" or more pipelines are setup/configured to accommodate/conform to the network dynamic/change nature of real time data load or bandwidth/delay (i.e. network characteristics)).

Regarding Claim 17, Zahn discloses wherein an additional processing unit (see FIG. 2, a combined system of CPU 5" and memory 6") for the processing and/or transmission of time-synchronous data is used in sequence with the first and second processing units (see FIG. 2, a combined system of CPU 5" and memory 6" process the video data (i.e. processing of frame 103) in parallel sequence with first and second combined systems (i.e. processed frames 101 and 102); see page 9, last paragraph; see page 11, paragraph 1-2; see page 12, paragraph 2; see page 13, paragraph 4-5).

Regarding Claim 18, Zahn discloses wherein the time-synchronous data is gathered with one of mechanisms for acquiring visual data and speech data (see page 4, paragraph 3-8; see page 9, last paragraph; video data is collected/received by a apparatus 1 for obtaining/acquiring video data (i.e. image/visual data and audio/speech data).

7. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zahn and Sastry, and further in view of Muniere (US007095717B2).

Regarding Claim 5, Zahn discloses wherein the certain switching condition is whether at least one given parameter (see FIG. 2, switching/changing to CPU 5' or 5" is based on whether frame 101 is processed by CPU 5; see page 9, last paragraph; see page 11, paragraph 1-2; see page 12, paragraph 2; see page 13, paragraph 4-5).

Zahn does not explicitly disclose reaches at a predetermined value. However, Muniere teaches the certain switching condition (see FIG. 4, Switch 41) is whether at least one given parameter reaches at a predetermined value (see FIG. 3-4, switching is performed according to

meeting threshold/maximum High/low priority data counts; see col. 5, line 4-55; see col. 6, line 26-45).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide switching when reaching a predetermined value, as taught by Muniere in the combined system of Zahn and Sastry, so that it would provide guaranteeing a minimum time interval for transmission of data packets; see Muniere col. 6, line 40-45.

Second set of rejection

Claim Rejections - 35 USC § 102 (b)

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-13, 15, and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Ochi (U.S. 5,299,003).

Regarding Claim 1, Ochi discloses an apparatus (see FIG. 1; signal processing apparatus) for the transmission of time-synchronous data (see FIG. 1, transmission of video signals; see col. 6, line 26-30) from a sender (see FIG. 1, input terminal 10) to a receiver (see FIG. 1, output terminal 21) using a network (see FIG. 1; a network of input terminal 10, processing apparatus and output terminal 21), wherein the time-synchronous data is processed and transmitted at the sender as well as the receiver (see FIG. 1, the video signal is processed

and transmitted at input terminal 10 as well as the output terminal 21; see col. 5, line 55-60; see col. 6, line 20-45), the mechanism comprising:

a first processing unit (see FIG. 1, a combined system of first memory 12, transmitter 14 and third memory 16) composed of multiple subcomponents (see FIG. 1, first memory 12, transmitter 14 and third memory 16), each subcomponent being designed to process the time-synchronous data in a specific and different way (see FIG. 1, first memory 12 process the video signal in specific/particular and different/dissimilar way/method (e.g. storing video data signal input from transmitter 11) from third memory 16 and transmitter 14; transmitter 14 process the video signal in specific/particular and different/dissimilar way/method (e.g. transmitting video data signal input from memory 12) from first and third memory 12, 16; third memory 16 process the video signal in specific/particular and different/dissimilar way/method (e.g. storing video data signal input from transmitter 14) from first memory 12 and transmitter 14; see col. 5, line 55 to col. 6, line 55);

a second processing unit parallel to the first processing unit (see FIG. 1, a combined system of second memory 13, transmitter 15 and fourth memory 17 is parallel to a combined system of first memory 12, transmitter 14 and third memory 16; see col. 5, line 55 to col. 6, line 55), composed of multiple subcomponents (see FIG. 1, second memory 13, transmitter 15 and fourth memory 17), each subcomponent being designed to process the time-synchronous data in a specific and different way (see FIG. 1, second memory 13 process the video signal in specific/particular and different/dissimilar way/method (e.g. storing another video data signal input from transmitter 11) from fourth memory 17 and transmitter 15; transmitter 15 process the video signal in specific/particular and different/dissimilar way/method (e.g. transmitting video

data signal input from memory 13) from second and fourth memory 13,17; fourth memory 17 process the video signal in specific/particular and different/dissimilar way/method (e.g. storing video data signal input from transmitter 15) from second memory 13 and transmitter 15; see col. 5, line 55 to col. 6, line 55);

wherein the subcomponents of second processing unit are setup and adapted based on changed sender data rate or network characteristics (see FIG. 2a-h, memory 13,17 and transmitter 15 are configured/setup and fit/adapted for parallel storage and processing according to transmitting/sending data rate or network transmission characteristic; see col. 5, line 55 to col. 6, line 55) by configuring attribute parameters of the subcomponents (see col. 5, line 55 to col. 6, line 55; by setting/configuring timing parameters of the memory 13,17 and transmitter 15),

wherein data processing and transmission of the time-synchronous data is continued within the first processing unit during the setup and adaptation of the second processing unit (see FIG. 1, 2a-h, processing and transmission of video data is continue at t0 to t1, t2 to t3, and t4 to t5 within the combined system of first memory 12, transmitter 14 and third memory 16 during the configuration/setup and fitting/adaptation of a combined system of second memory 13, transmitter 15 and fourth memory 17; see col. 6, line 26 to col. 7, line 10);

a switch (see FIG. 1, Switch circuit 18) selecting between the first and second processing units (see FIG. 1, switching/changing/selecting between the combined system of first memory 12, transmitter 14 and third memory 16, and the combined system of second memory 13, transmitter 15 and fourth memory 17; see col. 6, line 6-55), the processing and transmission of the time-synchronous data initially being performed by the first processing unit (see FIG. 1, 2a-h, processing and transmission of video primarily/initially performed by the combined system of

first memory 12, transmitter 14 and third memory 16 at t0 to t1, t2 to t3, and t4 to t5) and after switching, the processing and transmission of the time-synchronous data is performed using the second processing unit (see FIG. 1, 2a-h, after switching processing and transmission of video data signal is processed by the combined system of second memory 13, transmitter 15 and fourth memory 17 at t1 to t2, t3 to t4, and t5 to t6) such that the processing and transmission of the time-synchronous data is performed within the second processing unit (see FIG. 1, 2a-h, such that the processing and transmission of video data signal is performed by the combined system of second memory 13, transmitter 15 and fourth memory 17); see col. 6, line 26 to col. 7, line 10).

Regarding Claim 2, Ochi discloses wherein the setup and adaptation of the second processing is started using a trigger event (see FIG. 3a-j, the configuration/setting-up and fitting/adaptation of a combined system of second memory 13, transmitter 15 and fourth memory 17 is began/stated using waveform up/down event; see col. 6, line 26 to col. 7, line 10).

Regarding Claim 3, Ochi discloses wherein the switching is performed after the completion of the setup and/or adaptation of the second processing unit (see FIG. 1, switching is performed after completion/ending of setup/configuration/setting and adaptation/fitting of the combined system of second memory 13, transmitter 15 and fourth memory 17; see col. 6, line 6-55).

Regarding Claim 4, Ochi discloses wherein the switching is performed after reaching a certain switching condition (see FIG. 2, switching is performed after reaching t1, t3, and/or t5 (i.e. condition) which triggers switching; see col. 6, line 6-55).

Regarding Claim 5, Ochi discloses the certain switching condition is whether at least one given parameter reaches at a predetermined value (see FIG. 2, switching condition is whether the time reaching t1, t3, and/or t5; see col. 6, line 6-55)

Regarding Claim 6, Zahn discloses wherein the time-synchronous data is processed in the first processing unit using a plurality of subcomponents (see FIG. 1, a combined system comprising first memory 12, transmitter 14 and third memory 16; see col. 5, line 55 to col. 6, line 26).

Regarding Claim 7, Ochi discloses wherein the subcomponents includes at least one of a memory buffer (see FIG. 1, a combined processing system comprising first memory 12 or third memory 16; see col. 5, line 55 to col. 6, line 26).

Regarding Claim 8, Ochi discloses wherein the time-synchronous data is processed in the second processing unit using a plurality of subcomponents (see FIG. 1, a combined system of second memory 13, transmitter 15 and fourth memory 17; see col. 5, line 55 to col. 6, line 26).

Regarding Claim 9, Zahn discloses wherein the subcomponents includes at least one of a memory buffer (see FIG. 1, a combined processing system comprising second memory 13 or fourth memory 17; see col. 5, line 55 to col. 6, line 26).

Regarding Claim 10, Ochi discloses wherein the subcomponents are connected during the setup (see FIG. 1, a combined system of second memory 13, transmitter 15 and fourth memory 17 are connected during the configuration/setups; see col. 5, line 55 to col. 6, line 26).

Regarding Claim 11, Ochi discloses wherein the first and second processing unit is initialized after the setup (see FIG. 1, a combined system of first memory 12, transmitter 14 and third memory 16, and a combined system of second memory 13, transmitter 15 and fourth

memory 17 are initialized/started/begin processing after the configuring/setting-up; see col. 5, line 55 to col. 6, line 26).

Regarding Claim 12, Ochi discloses wherein each of the subcomponents of the second processing unit is adapted to the other subcomponents (see FIG. 2, each second memory 13, transmitter 15 or fourth memory 17 is adapted/fit/adjust/corresponds to other second memory 13, transmitter 15 or fourth memory 17; or other first memory 12, transmitter 14 and third memory 16; see col. 5, line 55 to col. 6, line 26), or the changed data rate, or changed network characteristics (changing/switching data rate or network transmission characteristic; see col. 5, line 55 to col. 6, line 55).

Regarding Claim 13, Ochi discloses wherein after the switching process, the subcomponents of the first processing unit are de-attached from each other (see FIG. 1, after switching, first memory 12, transmitter 14 and third memory 16 are separated/de-attached from second memory 13, transmitter 15 or fourth memory 17; see col. 5, line 55 to col. 6, line 55).

Regarding Claim 15, Ochi discloses wherein after switching by the switch, the subcomponents of the first processing unit remain connected (see FIG. 1, after switching memory 12, transmitter 14 and third memory 16 are still connected; see col. 5, line 55 to col. 6, line 26).

Regarding Claim 18, Ochi discloses wherein the time-synchronous data is gathered with one of mechanisms for acquiring visual data and speech data (see FIG. 1; video data is collected/received by a apparatus for obtaining/acquiring video data (i.e. image/visual data and audio/speech data); see col. 5, line 55 to col. 6, line 26).

10. Claims 14, 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ochi in view of Sastry (US006694373B1).

Regarding Claim 14, Ochi discloses the second processing units is setup and after switching by the switch (see FIG. 1, second memory 13, transmitter 15 or fourth memory 17 are configured/setup, and after switching by the switch; see col. 5, line 55 to col. 6, line 55); and the subcomponents of the first processing unit (see FIG. 1, second memory 13, transmitter 15 or fourth memory 17) as set forth above in claim 1.

Ochi does not explicitly disclose "a plurality of the second processing units" and "the subcomponents of the first processing unit are included in one of the second processing units".

Sastry discloses a plurality of the second processing units is setup (see FIG. 8, DSP 803,504,805,806 are setup/configured/constructed) and after switching by the switch after switching by the switch, the subcomponents of the first processing unit are included in one of the second processing units (see FIG. 8, after switching by a switch 420/620, subcomponent 2 ADPCM (Adaptive Pulse Code Modulation for voice compressing) from DSP 801 (i.e. first processing unit) are now included in the DSP 803; see col. 6, line 55 to col. 7, line 10).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide "a plurality of the second processing units" and "the subcomponents of the first processing unit are included in one of the second processing units", as taught by Sastry in the system of Ochi, so that it would increase the support for the number of simultaneous calls/real-time data transmission and efficient resource allocation; see Sastry col. 3, line 15-30; see col. 7, line 5-12.

Regarding Claim 16, Ochi discloses wherein a second processing unit (see FIG. 1, a combined system of second memory 13, transmitter 15 and fourth memory 17 are configured/setup, and after switching by the switch; see col. 5, line 55 to col. 6, line 55) are setup and adapted based on changed data rate and network characteristics (see FIG. 2a-h, setup/configured and fit/adapted for parallel storage and processing according to transmitting/sending data rate and network transmission characteristic; see col. 5, line 55 to col. 6, line 55).

Ochi does not explicitly disclose "a plurality of the second processing units".

Sastry discloses a plurality of the second processing units is setup (see FIG. 8, DSP 803,504,805,806 are setup/configured/constructed; see col. 6, line 55 to col. 7, line 10).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide "a plurality of the second processing units", as taught by Sastry in the system of Ochi, so that it would increase the support for the number of simultaneous calls/real-time data transmission and efficient resource allocation; see Sastry col. 3, line 15-30; see col. 7, line 5-12.

Regarding Claim 17, Ochi discloses the processing and transmission of time-synchronous data is used in sequence with the first and second processing units (see FIG. 2, a combined system of memory 12, transmitter 14 and memory 16 process the video data (i.e. processing of video) in parallel sequence with second combined system memory 13, transmitter 15, memory 17; see col. 5, line 55 to col. 6, line 55).

Ochi does not explicitly disclose "an additional processing unit".

Sastry discloses wherein an additional processing unit (see FIG. 1, DSP-D 439) for the processing and transmission of data is used in sequence with the first and second processing units (see FIG. 2, processing and transmission of data is used in parallel sequence with DSP-S 431 and DSP 432; see col. 6, line 55 to col. 7, line 10).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide "a plurality of the second processing units", as taught by Sastry in the system of Ochi, so that it would increase the support for the number of simultaneous calls/real-time data transmission and efficient resource allocation; see Sastry col. 3, line 15-30; see col. 7, line 5-12.

Response to Declaration Under 37 CFR 1.132

11. The declaration under 37 CFR 1.132 filed 2-1-2008, by Koichi Funaya (hereinafter refers to Funaya), is insufficient to overcome the rejection of claims 1-18 based upon insufficient disclosure under 35 U.S.C. 112, first paragraph and Zahn, Sastry and Muniere under 35 U.S.C 103 as set forth in the last Office action because:

(1) It refer(s) only to the system described in the above referenced application and not to the individual claims of the application. Thus, there is no showing that the objective evidence of nonobviousness is commensurate in scope with the claims. See MPEP § 716.

Funaya discloses "the invention disclosed therein relates to a **specification** of a method which allows for changing components…this invention is that it can be realized in software and hardware…based on specific requirement of the application (e.g. **video conference**) or device (e.g. **mobile phone**)…" on page 2-3.

In response, Funaya opinion is based on applicant specification, not the claim, since the opinion is directed to the application such as video conference or mobile phone, which is not recited in the claim. Reciting the use of "hardware" or "software" in the specification does not automatically enable the detailed structure of the claimed invention.

(2) It include(s) statements which amount to an affirmation that the claimed subject matter functions as it was intended to function. This is not relevant to the issue of nonobviousness of the claimed subject matter and provides no objective evidence thereof. See MPEP § 716.

Funaya discloses "it would mean to specify disconnection the subcomponents are to be done automatically by JMF…if some subcomponents should be re-used for other purposes and in order to free resources, a dedicated disconnected will be helpful. This would also release the implementation from additional performance requirement for synchronization and event-handling…avoid circuit feedback problems or to reduce energy consumption and heat problems…the re-use in the new processing chain would avoid the waiting time for setting up …" in page 2-3.

In response, Funaya opinion describes the list of detailed of intended use of the invention where the invention provides advantages/benefits, yet it fails to disclose that the claimed invention would be clearly understood by those skilled in the art without proper enabling disclosure. By describing the list of intended use of the invention and the disclosing only "hardware" or "software" in the specification, is not sufficient to overcome the rejection set forth above.

(3) It include(s) statements that are **contradiction** to each other. For example, in paragraph 2-4 on page 2-3, Funaya opinion describes "why" or "how" the applicant invention would be obvious to one skilled in the art in attempt to overcome U.S.C. 112, 1st paragraph rejection. In particular, Funaya recites, "*as far as I can observe, existing chipset could easily support the proposed method*", yet, at the same time Funaya opinion recites, in paragraphs 5-9, "why" or "how" the applicant invention is not obvious over Zahn in view of Sastry in attempt to overcome U.S.C. 103(a) rejection. Thus, it is clear that Funaya opinion is not sufficient to overcome the rejection since Funaya option recites first proposed method of the applicant can easily be done utilizing existing chipset (i.e. obvious to one skilled in the ordinary art), and at the same time proposed method is not obvious in view of prior arts. Clearly, the opinion evident provided by Funaya contradicts to each other.

(4) It includes statements "*Koichi Funaya declares….during a period form April 1989 to April 2001, I was employed by NEC,... during the period form April 2001 to December 2004, I was employed by Network Development Labs,... during the period from January 2005 to June 2006, I was employed by Infineon Technologies, ...since June 2006, I have been employed by Network Research Division, NEC Laboratories as CPO,...I graduated from Massachusetts Institute of Technology with Mater of Science Degree in Aeronautic and Astronautics in 1988...and from University of Tokyo with Master of Science degree at school of engineering in 1989…*" in page 1, paragraph 1;.

After analyzing the skill level and qualifications of Funaya, it is clear that Funaya has over 19 years experiences and two master degrees, which qualifies Funaya as an expert, not the person of ordinary skill in the art (hereinafter "routineer"). Funaya's skill level is higher than that

required by the routineer. Routineer would not understand and make use of a particular application recited claim 13 and 14 without proper written disclosure. One can clearly see this fact by reviewing Funaya own statement in the disclosure "…*the switching process is* ***quite straight-forward****...can be realized in many ways*…" in page 3, paragraph 4. Only an expert Funaya, not routineer in the art, can easily declare such statement that the claim 13 and claim 14 without proper enabling disclosures recited in the applicant specification. Therefore, the Funaya declaration would not be probative as to the amount of experimentation required by a routineer in the art to implement the invention. (see MPEP 716, 2164.06 III).

In view of the foregoing, when all of the evidence is considered, the totality of the rebuttal evidence of nonobviousness fails to outweigh the evidence of obviousness.

Response to Arguments

12. Applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection.

Regarding claims 13 and 14, the applicant argued that, "…regarding claim 13…the specification recites on page 7, lines 27-28 that "***The switch can hereby be realized as hardware or software***"…arguing that "as would be clearly understood by those of ordinary skill in the art, disconnection (and re-connection) of the codec, filter and packetizer could also be realized with either hardware or software switches…regarding claim 14…"a plurality of the second processing units" and that "the subcomponents of the first processing unit are included in one of the second processing units…claim quite clearly contemplates a plurality of second processing unit and when the subcomponents of the first processing unit are incorporated into one of the second

processing units, one of ordinary skill in the art would understand that parallel processing is performed by at least two of the plurality of second processing units…Funaya states "claim refers to the variant, where some of the original subcomponents…second processing units…This would allow for both resources efficient and speed-efficient implementation.." in page 6-8.

In response to applicant's argument, t**he examiner respectfully disagrees** with the argument above.

Regarding claim 13, one skilled in the ordinary art would see that by disclosing the switch is "hardware" or "software" in the specification clearly is not enabling disclosure for the claimed invention "**after switching by the switch, the subcomponents of the first processing unit** (i.e. CODEC, FILTER and PACKETIZER) **are de-attached from each other**"

1) since "the switch" and "CODEC, FILTER and PACKETIZER" separated components, and thus having a hardware or software "switch" has nothing to do with "CODEC 6a, FILTER 6b and PACKETIZER 6c" are de-attached/disconnect from each other. Clearly, one skilled in the ordinary would not know how to de-attached/disconnect CODEC 6a, FILTER 6b and PACKETIZER 6c from each other after the switch without enabling disclosure;

2) As shown in applicant specification FIG. 3, after switching by switch 5 from the first processing unit 3 to the second processing unit 4, the switch is now connecting with the second processing unit 4. Thus, it is also clear that having a hardware or software "switch" has nothing to do with "CODEC 6a, FILTER 6b and PACKETIZER 6c" in the first processing unit 3 since the switch is not even connected to "CODEC 6a, FILTER 6band PACKETIZER 6c" after switching to second processing unit 4. Clearly, one skilled in the ordinary would not know how

to de-attached/disconnect CODEC 6a, FILTER 6b and PACKETIZER 6c of first processing unit 3 from each other when the switch is not even connected to them without enabling disclosure.

Since the applicant argued that "as would be clearly understood by those skilled in the art", it clear that applicant is admitting the specification fails to support enabling disclosure for the claimed invention. Examiner agrees with the applicant admission since applicant referred page and lines or any other pages fail provide enabling support for the claimed invention.

As set forth above, the claimed invention would not be clearly understood by those skilled in the art. The arguments of counsel cannot take the place of evidence in the record (see MPEP 716.01(c) II).

Since applicant fails to clearly point out the enabling reference in the specification where the claimed invention is supported, and the claimed invention would not be clearly understood by those skilled in the art, examiner sustains the assumption, for the purpose of the examination, "in light of the applicant disclosure" *that after switching, the first processing subcomponents (6a', 6b',..) are de-attached/separated from the second processing subcomponents (7a', 7b',...).*

Regarding claim 14, first, applicant misunderstood the rejection since the issue is, as precisely stated, "**the** subcomponents of the first processing unit (i.e. CODEC 6a, FILTER 6b and PACKETIZER 6c) **are included in one of the second processing units (i.e. second processing unit 4)** while at least one of the second processing units 4 already has it own subcomponents (i.e. CODEC 6a, FILTER 6b and PACKETIZER 6c). Clearly, one skilled in the ordinary would not know how to incorporate CODEC 6a, FILTER 6b and PACKETIZER 6c from first processing unit 3 to at least one of the second processing units 4 without enabling disclosure.

Since the applicant argued that "as would be clearly understood by those skilled in the art", it clear that applicant is admitting the specification fails to support enabling disclosure for the claimed invention. Examiner agrees with the applicant admission since applicant referred page and lines or any other pages fail provide enabling support for the claimed invention.

As set forth above, the claimed invention would not be clearly understood by those skilled in the art. The arguments of counsel cannot take the place of evidence in the record (see MPEP 716.01(c) II).

In view of the above, it is clear that applicant fails to clearly point out the enabling reference in the specification where the claimed invention is supported, and the claimed invention is not clearly understood by those skilled in the art.

Regarding Funaya option, the opinion is insufficient as set forth above in paragraph 10.

Regarding claims 1-18, **the applicant argued that,** "…MPEG and HDTV… Zahn does not disclose transmission of time-synchronous data and certainly does not disclose transmission of data using **a network**… This process is not real time….the point here is that the claimed invention is not a NLE system of Zahn type…Mr. Funaya notes that Zhan is directed to non-liner video editing which, by definition, is not time-synchronous transmission over a network… DSP load sharing scheme of Sastry is not the same or analogous to the claimed invention…Mr. Funaya notes again the claim 1..Zahn does not transmit any data but operates on a single machine…as to claim 2, Mr. Funaya notes that…Zahn does not change the parameters of a video editing unit after setup…as to claim 3, but Zahn switches before setup since the timing problems of component setup time do not matter for video editing…Sastry do not cover the problem of setup time at all…" in page 8-13.

In response to applicant's argument, t**he examiner respectfully disagrees** with the argument above.

In response to applicant's arguments, the recitation (**i.e. a sender, a receiver, and a network**) has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

Even if the limitation in the preamble were considered,

Zahn discloses an apparatus (see FIG. 1,2; apparatus 1) for the transmission of time-synchronous data (see FIG. 3, video signal 50; see page 4, paragraph 3-8; see page 9, last paragraph; real time/synchronous video signal utilizing MPEG or HDTV) from a sender to a receiver using a network (see page 4-6; a video signal must transmit from a transmitter to a receiver/customer over a network), wherein the time-synchronous data is processed and transmitted at the sender as well as the receiver (see FIG. 1, 2,4,5, the video data is processed at transmitter or receiver/customer; see page 9, last paragraph).

Also, Sastry discloses an apparatus (see FIG. 2, server 220/230/260; see FIG. 3, server 310; see FIG. 4,6; server 405/605) for the transmission of time-synchronous data (see FIG. 2, real time data; see col. 3, line 29-31, 48-51, 62-67) from a sender (see FIG. 2, sending/transmitting client 241-244/251-254) to a receiver (see FIG. 2, receiving client 251-254/241-244) using a network (see FIG. 2, using network 210), wherein the data is processed and

transmitted at the sender as well as the receiver (see FIG. 2,3,4,6, server 310 process and transmitted to sending client 241-244 as well as the receiving client 251-254; see col. 3, line 32 to col. 4, line 10).

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., **the real time process, PCI, MPEG, HDTV, NLE system**) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Even if this limitation "real time process" is claimed, Zahn still discloses the real time procession of MPEG/HDTV video packets.

Also, one skilled in the ordinary art will clearly see that MPEG/HDTV is a real time packet data that is transmitted from a sender (i.e. MPEG/HDTV generator/transmitter) and to a receiver (i.e. MPEG/HDTV receiver/player) over a network. The "network" is consisted of sender, receiver and the apparatus that process the MPEG/HDTV video packets. Applicant has not claimed any specification with regards to sender, receiver and network. When MPEG/HDTV video packets are created, it is clear that there is a sender/transmitter/generator, a receiver/player, and a network where transmission of the MPEG/HDTV video packets occurs.

Applicant is arguing the broad claimed limitation "time-synchronous data" does not equate to a video/audio data such as "MPEG or HDTV". First, "time-synchronous data" is a broad term, and every data that are processed "time-synchronously" can be asserted as time-synchronous data. Second, applicant own specification recites "audio/video" senders in background of the invention. Thus, applicant augments and the specification does not agree.

Moreover, one skilled in the art would clearly see that time-synchronous video data is being represented by MPEG or HDTV data signal. Thus, arguing MPEG and HDTV data signals are not "time-synchronous" data is clearly an error.

In response to applicant's argument that "Sastry is not the same nonanalogous art", it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide a switch, as taught by Sastry in the system of Zahn, so that it would increase the support for the number of simultaneous calls/real-time data transmission and efficient resource allocation; see Sastry col. 3, line 15-30; see col. 7, line 5-12.

In repose to applicant argument, identical applicant claimed invention, the combined system of Zahn and Sastry discloses operating the video data and transmitting the video as set forth below.

In particular, Zahn discloses the processing and **transmission** of the time-synchronous data is performed using the second processing unit (see FIG. 1-3, processing and transmission of real time data packet (e.g. continue data packet 102) is processed by CPU 5'; see page 4, paragraph 3-4, 8 page 8, paragraph 3-7; page 11, paragraph 1 to page 12, paragraph 3; see page 13, paragraph 5-6, last paragraph) such that the processing and transmission of the time-synchronous data is performed within the second processing unit (see FIG. 1-3, the pr processing and transmission of real time data packet (e.g. continue data packet 102) is processed by CPU 5''

see page 4, paragraph 3-4, 8 page 8, paragraph 3-7; page 11, paragraph 1 to page 12, paragraph 3; see page 13, paragraph 5-6, last paragraph).

Sastry also discloses the processing and transmission of the time-synchronous data is performed using the second processing unit such that the processing and transmission of the time-synchronous data is performed within the second processing unit (see FIG. 4,6,8, processing and transmission of real time data is performed using the DSP-D (or any another DSP besides DSP-S) such that processing and transmission of the real time data is performed within DSP-D (or another DSP); see col. 4, line 39-62; see col. 5, line 10-26, 36-56; see col. 6, line 12-20l; see col. 6, line 55 to col. 7, line 11).

Regarding Claim 2, Zahn discloses wherein the setup and adaptation of the second processing is started using a trigger event (see FIG. 1, PULL request 1 is used to being processing video frames in CPU 5'; see page 11, paragraph 1-2; see page 12, paragraph 2; see page 13, paragraph 4).

Regarding Claim 3, Zahn discloses wherein the switching is performed after the completion of the setup and/or adaptation of the second processing unit (see FIG. 2, switching/changing to CPU 5' after setup/configuration/setting CPU 5'; see page 9, last paragraph; see page 11, paragraph 1-2; see page 12, paragraph 2; see page 13, paragraph 4-5).

Regarding claim 5, t**he applicant argued that,** "…Muniere cannot be combined with Zahn to make a workable system. The two are in entirely different technical fields…There is no basis in fact for the conclusion of obviousness…" in page 14-16.

In response to applicant's argument, t**he examiner respectfully disagrees** with the argument above.

In response to applicant's argument that "*the two are in entirely different technical fields*" (i.e. nonanalogous art), it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, the combined system of Zahn, Sastry and Muniere and the applicant's invention are concerted with the certain switching condition (see FIG. 4, Switch 41) is whether at least one given parameter reaches at a predetermined value (see FIG. 3-4, switching is performed according to meeting threshold/maximum High/low priority data counts; see col. 5, line 4-55; see col. 6, line 26-45). Thus, it is clear that Muniere is the analogous art.

In response to applicant's argument, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to IAN N. MOORE whose telephone number is (571)272-3085. The examiner can normally be reached on 9:00 AM- 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Doris To can be reached on 571-272-7629. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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